Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure
Inventor(s): Wan Yen Teoh and Che Seong Law
Case No.: 03-11 (SE0099), Sheet 1/9

V_{CG}

106

108

104

V_D

V_S

102

110

112

114

100

FIG. 1 (Prior Art)

V_{Sub}

103

122

100

120

126

124

FIG. 2 (Prior Art)

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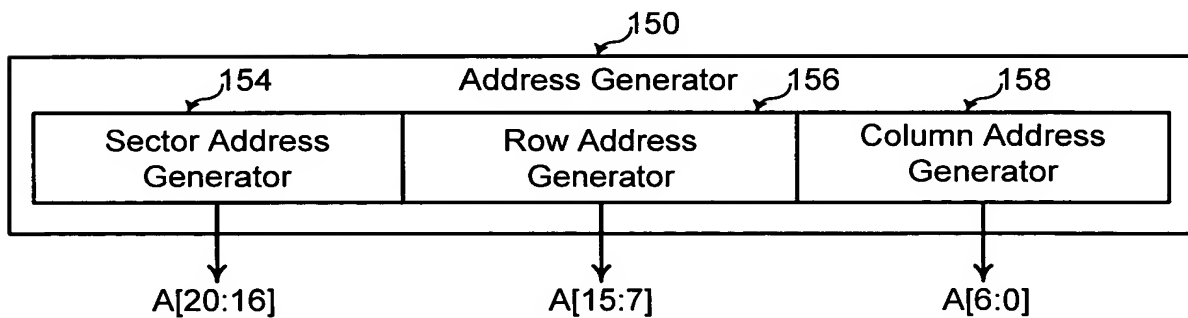Case No.: 03-11 (SE0099), Sheet 2/9

FIG. 3 (Prior Art)

FIG. 4 (Prior Art)

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FIG. 5 (Prior Art)

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FIG. 6

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190

178

176

Heater with Timer

Burn-In Board

174

160

Flash Memory Device

A[20:0]

180

182

164

Word-line
Clock Signal
Generator

Address Signal
Driver

A[20:0]

170

Address
Generator
(Binary Sequence)

150

Bit-line Voltage
Generator

Driver Board

FIG. 7

Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure
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FIG. 8

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200

178

176

Heater
with Timer

Burn-In Board

174

160

Flash Memory Device

A'[20:0]

180

Word-line
Clock Signal
Generator

164

Address Signal
Driver

182

A'[20:0]

Bit-line Voltage
Generator

170

Binary to Gray
Code Converter

204

A[20:0]

Address
Generator
(Binary Sequence)

150

Driver Board

FIG. 9

Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure
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Start

Place burn-in board with flash memory device in heating chamber and set timer. —212

Generate one address A[20:0] in binary sequence. —214

Convert A[20:0] in binary sequence to A'[20:0] in Gray Code sequence. —216

Apply test voltage signals and address signals A'[20:0] in Gray Code sequence to burn-in board. —218

HTOL time period elapsed? —220

NO

YES

End

FIG. 10

302 Binary Sequence A2 A1 A0	306 # of Bit Transitions	304 Gray Code A'2 A'1 A'0	308 # of Bit Transitions
0 0 0		0 0 0	
0 0 1	1	0 0 1	1
0 1 0	2	0 1 1	1
0 1 1	1	0 1 0	1
1 0 0	3	1 1 0	1
1 0 1	1	1 1 1	1
1 1 0	2	1 0 1	1
1 1 1	1	1 0 0	1
0 0 0	3	0 0 0	1

FIG. 11

Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure
Inventor(s): Wan Yen Teoh and Che Seong Law
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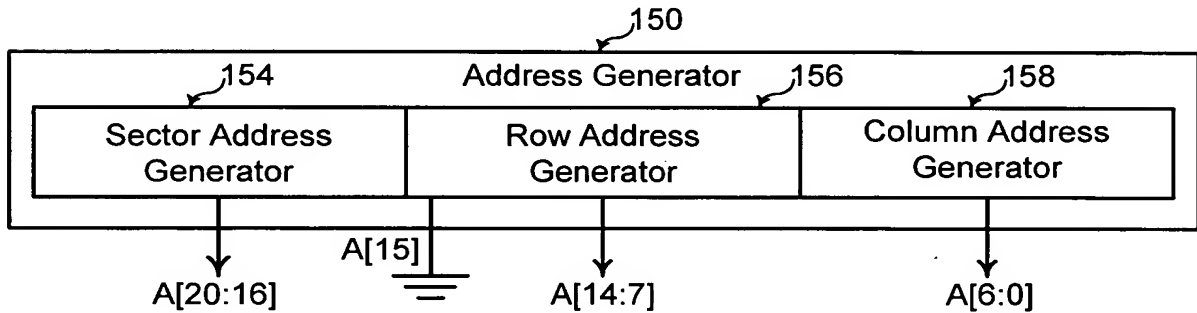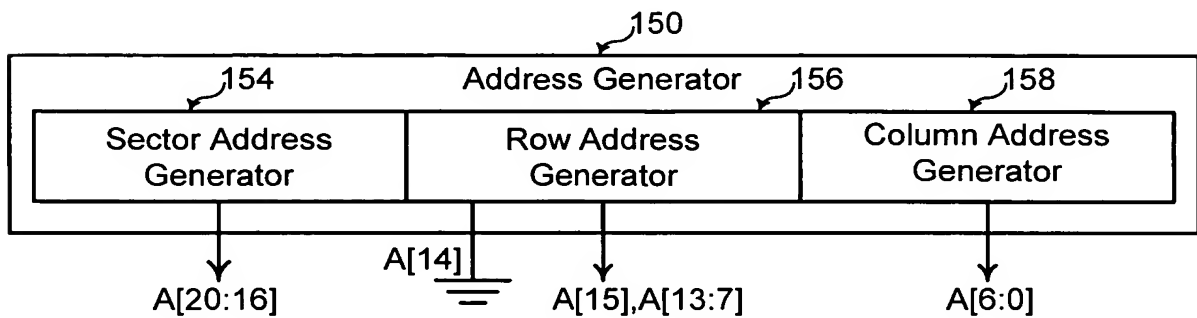| 312 Experimental Condition	314 Row Location for Charge Gain Failure	316 Quantity Failed
322 Ascending Binary	Row 0, Sector 0	1/90 Units (1 bit failed)
324 Descending Binary	Row 511, Sector 31	2/90 Units (1 bit failed)
326 Descending Binary with A15 Grounded.	Row 495, Sector 31	4/90 Units (1 bit failed)
328 Descending Binary with A14 Grounded.	Row 503, Sector 31	2/90 Units (1 bit failed)
330 Gray Code	No Failure	No Failure

FIG. 12

150

Address Generator

| 154 Sector Address Generator | 156 Row Address Generator | 158 Column Address Generator |

A[20:16]   A[15]   A[14:7]   A[6:0]

FIG. 13

150

Address Generator

| 154 Sector Address Generator | 156 Row Address Generator | 158 Column Address Generator |

A[20:16]   A[14]   A[15],A[13:7]   A[6:0]

FIG. 14